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PERFORMANCE ANALYSIS OF HIGH EFFICIENCY LOW DENSITY PARITY-CHECK CODE DECODER FOR LOW POWER APPLICATIONS

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ABSTRACT

To propose a low power, high efficient Low Density Parity-Check Code (LDPC) Decoder Architecture for error detection and non-complex applications. LDPC codes have been adopted in latest wireless standards such as electronic devices communications since they possess superior error-detecting and correcting capabilities. As technology scales, memory devices become larger and more powerful and low power consumption based error correction codes are needed. In this method we developed the Good error correcting performance enables efficient and reliable communication. The output from variable unit is stored in the storage elements which received the address sequence from the address generator module. The method is to improve to optimize one recurrent task that is performed within each decoding and check the verification is performed in order to confirm the validity of the obtained code block and hence decide whether to continue or halt the decoding process.

Keywords:

Common subexpression (CS), complexity reduction, encoding complexity, low-density parity-check (LDPC) encoding, matrix inversion, multi-Gbps throughput rate, quasi-cyclic (QC) LDPC, VLSI architecture.

1. INTRODUCTION

Coded modulation is a bandwidth-efficient scheme that integrates channel coding and modulation into one single entity to improve performance with the same spectral efficiency compared to encoded modulation. Low-density parity-check (LDPC) codes are the most powerful error correction codes (ECCs) and approach the Shannon limit, while having a relatively low decoding complexity.

Therefore, the idea of combining LDPC codes and bandwidth-efficient modulation has been widely considered. In this thesis we will consider LDPC codes as an Error Correcting Code and study it's performance with BPSK system in AWGN environment and study different kind of characteristics of the system. LDPC system consists of two parts Encoder and Decoder. LDPC encoder encodes the data and sends it to the channel.

The LDPC encoding performance depends on Parity matrix behavior which has characteristics like Rate, Girth, Size and Regularity. We will study the performance characteristics according to these characteristics and find performance variation in term of SNR performance. The decoder receives the data from the channel and decodes it. LDPC decoder has characteristics like time of iteration in addition all parity check matrix characteristics. We will also study the performance according to these characteristics. The main objective of this thesis is to implement LDPC system in FPGA. LDPC Encoder is implementation is done using Shift-Register based design to reduce complexity. LDPC decoder is used to decode the information received from the channel and decode the message to find the information. In the decoder we have used Modified Sum Product (MSP) Algorithm to decode, In the MSP we have used some quantized values to decode the data using Look Up Table (LUT) approximation. Finally we compare the SNR performance of theoretical LDPC system's with FPGA implemented LDPC system's performance.

1.1 ERROR DETECTION AND CORRECTION SCHEMES

Communication system transmits data from source to transmitter through a channel or medium such as wired or wireless. The reliability of received data depends on the channel medium and external noise and this noise creates interference to the signal and introduces errors in transmitted data. Shannon through his coding theorem showed that reliable transmission could be achieved only if data rate is less than that of channel capacity. The theorem shows that a sequence of codes of rate less than the channel capacity have the capability as the code length goes to infinity.

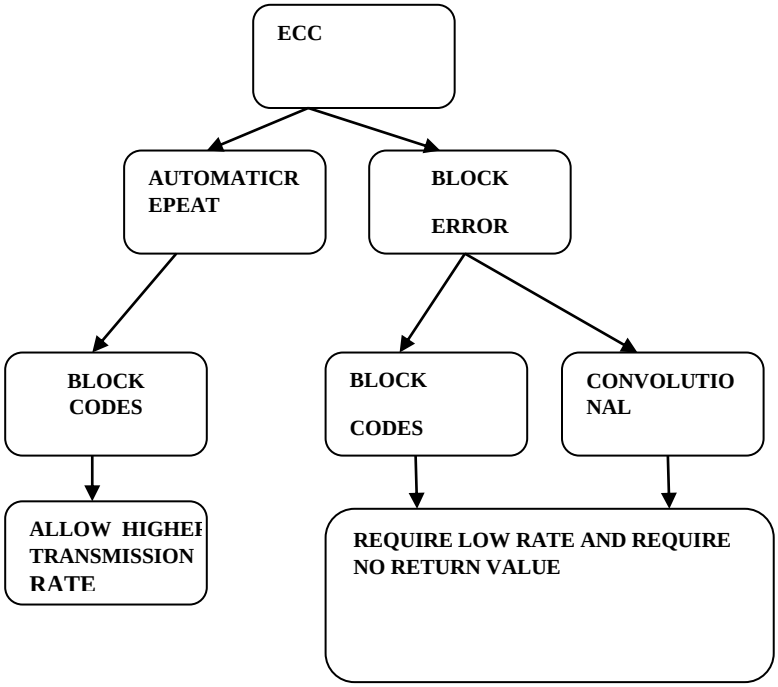


Fig 1.1 Fault Error Technique

Error detection and correction can be achieved by adding redundant symbols to the original data called as error correction and correction codes (ECCs).Without ECCs data need to retransmitted if it could detect there is an error in the received data. ECC are also called as for error correction (FEC) as we can correct bits without retransmission. Retransmission adds delay, cost and wastes system throughput. ECCs are really helpful for long distance one way communications such as deep space communication or satellite communication. They also have application in wireless communication and storage device.

2. RELATED WORKS

A high data-rate low-density parity-check (LDPC) decoder, suitable for the 802.11n/ac (Wi-Fi) standard. The innovative features of the proposed decoder relate to the decoding algorithms and the interconnection between the processing elements. The reduction of the hardware complexity of decoders based on the min-sum (MS) method comes at the cost of performance degradation, especially at high-noise regions. We introduce more accurate approximations of the log sum-product algorithm that also operate well for low signal-to noise ratio values. Telecommunication standards, including Wi-Fi, support more than one quasi-cyclic LDPC codes of different characteristics, such as code-word length and code rate, .technique derives networks, capable of supporting a variety of codes and efficiently realizing connectivity between a variable numbers of processing units, with a relatively small hardware overhead over the single-code case.

As a demonstration of the proposed technique, we implemented a reconfigurable network based on barrel rotators, suitable for LDPC decoders compatible with Wi-Fi standard**.** The problem of finding efficiently the first k minimum or maximum values is generally met in many application fields, such as error control coding. More specifically, optimized solutions for the selection of the two or three smallest elements out of a given set of numbers are greatly needed for the design of high-speed Low-Density Parity-Check (LDPC) decoders, as this min-search can be the bottleneck. This project to tackle current limitations by proposing a novel algorithm for solving this problem, where the searching is based on scanning from the most significant bit (MSB) to the least significant bit (LSB) of each input data. A design mapped to reconfigurable logic and a software tool for the automatic generation of synthesizable VHDL codes.

3. PROPOSED METHOD

In the proposed method we improve the error-correction performance at very low complexity.LDPC codes are finding the number of user in applications requiring reliable and highly efficient information transfer over

bandwidth or return channel-constrained links in the presence of corrupting noise. The decoder designed using our method consists of processing elements-Check data Unit. To overcome such limitation, hybrid architecture circuits which combines the features of check the data and variable node, may be used in future.The standard model has improved in speed and if speed will increase, the output low error technique has proposed in low complex design

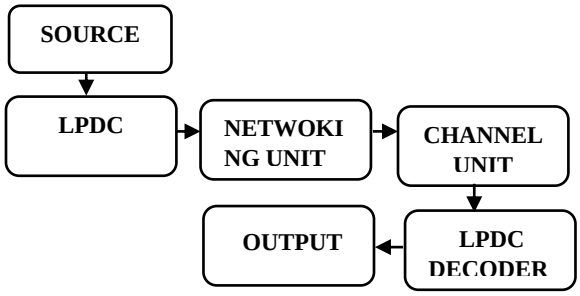


Fig 3 Proposed Block diagram

4. ANALYSIS AND DESIGN OF COST-EFFECTIVE, HIGH-THROUGHPUT LDPC DECODERS

introduces a new approach to cost-effective, high-throughput hardware designs for low-density parity-check (LDPC) decoders. The proposed approach, called nonsurjective finite alphabet iterative decoders (NS-FAIDs), exploits the robustness of message-passing LDPC decoders to inaccuracies in the calculation of exchanged messages, and it is shown to provide a unified framework for several designs previously proposed in the literature. NS-FAIDs are optimized by density evolution for regular and irregular LDPC codes, and are shown to provide different tradeoffs between hardware complexity and decoding performance. Two hardware architectures targeting high-throughput applications are also proposed, integrating both Min-Sum (MS) and NS-FAID decoding kernel.

4.1 REDUCED-COMPLEXITY TRELLIS MIN-MAX DECODER FOR NON-BINARY LDPC CODES

a novel algorithm and corresponding reducedcomplexity decoder architecture are proposed for decoding the trellis min-max NB-LDPC code. This proposal reduces the number of messages exchanged between check node and variable node as well as the hardware complexity. Thus, the memory requirement and the wiring congestion is decreased, which increases the throughput of the decoder with a negligible error-correcting performance loss a novel m TEC-TMM algorithm and corresponding decoder architecture are proposed for decoding the NB-LDPC codes. The results demonstrate that the proposed m TEC-TMM layered decoder greatly reduces both the CNU complexity, the wiring congestion and the memory requirements with negligible performance loss, compared to conventional trellis min-max decoders. However, a large memory requirement is required to store the CNU output messages.

4.2 FPGA IMPLEMENTATION OF PARITY CHECK MATRIX BASED LOW DENSITY PARITY CHECK DECODER

2018Low Density Parity Check (LDPC) error correction decoders have become popular in diverse communication systems, owing to their strong error correction performance and their suitability to parallel hardware implementation. Low Density Parity Check Decoder is a class of Forward Error Correction Codes. The parameterization of a particular LDPC code is defined by its Parity Check Matrix. Parity Check matrix which describes the specific logical combination of the transmitted message bits into parity checks. PCMs are sparse matrices having far more zero entries than nonzero. It allows LDPC codes to be iteratively decoded using a low complexity message passing algorithm. The implementation of these components are done on FPGA kit to improve the error correction performance of communication system.

4.3 LOW-COMPLEXITY, HIGH-SPEED MULTI-SIZE CYCLIC-SHIFTER FOR QUASI-CYCLIC LDPC DECODER

Quasi-cyclic low-density parity check (QC-LDPC) codes are being widely used in communication standards, and the decoder of QC-LDPC codes requires a unique type of rotator. The unique rotator, called a multi-size cyclic-shifter (MSCS), should be able to rotate data with various sizes, and many structures have been proposed for the operation. A low-complexity, high-speed MSCS structure is proposed, in which a part of the previous smallest structure is replaced with a structure with less delay and comparable

area. The synthesis results present that the proposed structure achieves not only the highest speed but also the lowest complexity after synthesis. a low-density parity-check (LDPC) code has been widely used because of high error correcting capability, and there are many variations including a quasi-cyclic LDPC (QC-LDPC) code. A QC-LDPC code creates a relatively simple encoder/decoder circuit and has been exploited in many communication standards. The code structure of a QC-LDPC code has a cyclic property, so the decoding process of a QC-LDPC code is related to a rotation operation. rotation size.

4.4 A 21.66GBPS NON-BINARY LDPC DECODER FOR HIGH-SPEED COMMUNICATIONS

2017Compared to binary Low-Density Parity-Check (LDPC) codes, Non-Binary LDPC (NB-LDPC) codes have better error correction performance under short to moderate block lengths or high-order modulations. Traditional min-sum based soft decoding algorithms for NB-LDPC codes suffer from large computational complexity, which leads to inefficient hardware implementations.However, efficient hardware implementations based on the MWBRB algorithm have not been investigated. In this work, an Improved Layered MWBRB algorithm is first proposed, which results in faster convergence rate than the MWBRB algorithm. Then, an ultra-high-throughput low-complexity decoder architecture with an efficient partially parallel processing schedule is also presented. Finally, the proposed architecture is coded with RTL and synthesized under the TSMC 90nm CMOS technology. In order to reduce the complexity, the Extended Min-Sum (EMS), Min-Max (MM), simplified min-sum and Trellis based EMS (T-EMS) algorithms were developed.

5. LOW-DENSITY PARITY-CHECK CODES

Low-density parity-check (LDPC) codes are forward error-correction codes, first proposed Here we will only consider binary messages and so the transmitted messages consist of strings of 0's and 1's. The essential idea of forward error control coding is to augment these message bits with deliberately introduced redundancy in the form of extra check bits to produce a codeword for the message. These check bits are added in such a way that code words are sufficiently distinct from one another that the transmitted message can be correctly inferred at the receiver, even when some bits in the codeword are corrupted during transmission over the channel. The simplest possible coding scheme is the single parity check code (SPC).

5.1 MATRIX METHOD OF LDPC CODE

And logarithmic computations are necessary to compute the check node. The Min-Sum (MS) algorithm, interchanges the product term with the minimum value. Even though performance is reduced, the hardware complexity of the BP algorithm is significantly minimized, by replacing complex computations of check nodes with simple summation and comparison operations. The min-sum algorithm provides a less sensitivity in decoding performance under finite word-length implementations and do not require channel information. Due to this advantage, MS algorithm is widely used.

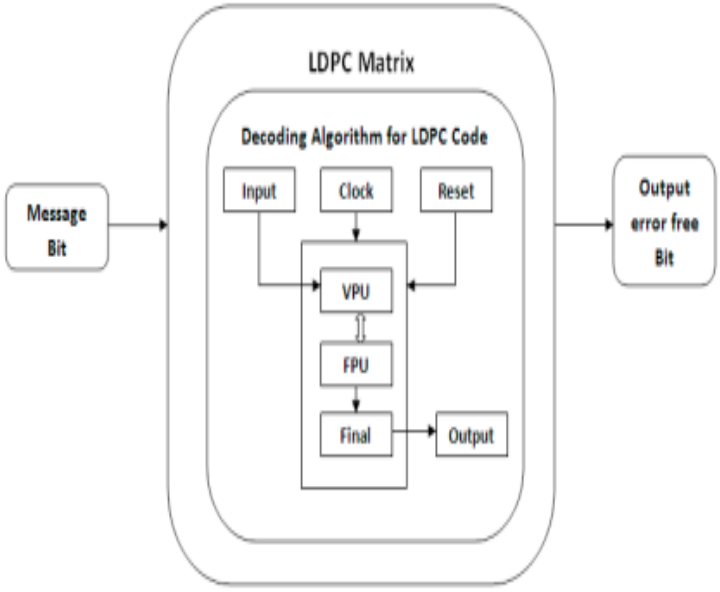


Fig 5.1 Generic block diagram of decoder for LDPC codes.

5.2 BINARY LPDC DECODER

An ace in *H* indicatesconnection between the corresponding variable and checknodes of the Tanner graph. Message-passing (MP) algorithmsfor decoding LDPC codes operate by iteratively exchanginginformation along the edges of the Tanner graph, betweenconnected

variable and check nodes. There are a variety ofMP decoding algorithms, such as the sum-product (SP),log-SP, and min-sum (MS) algorithm.For LDPC-BC decoders, the major design challenge is thecomplex interconnection. For high code rate LDPC-BCs, moreedges are connected to a check node such that large sortrequired to find the minimum value in the NMS algorithm.Furthermore, a fully parallel design causes large silicon areaand low chip density owing to a large amount of messages exchangingbetween CNUs and VNUs in one iteration. In itreported the size of decoder is determined by routing congestionand not by the computation logic gate count in the pastyears.

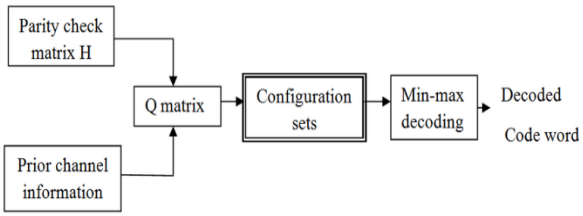
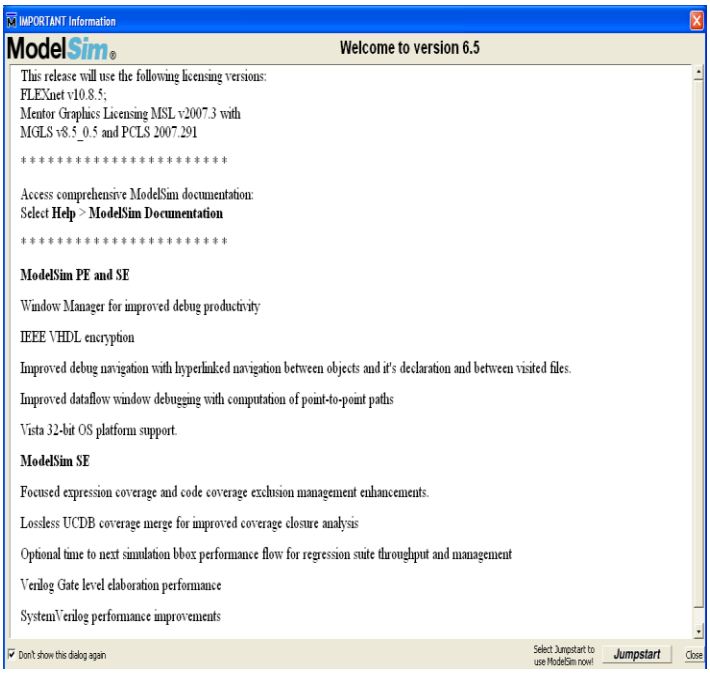


Figure 5.2 System Block Diagram of Non-Binary LDPC Decoder

6. SOFTWARE ANALYSIS

Model Sim PE, our entry-level simulator, offers VHDL, Verilog, or mixed-language simulation. Coupled with the most popular HDL debugging capabilities in the industry, Model Sim PE is known for delivering high performance, ease of use, and outstanding product support.



Tool Structure and Flow

The diagram below illustrates the structure of the Model Sims tool, and the flow of that tool as it is used to verify a design.

7. SIMULATION RESULTS

```
Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: No path found

Timing Details:
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All values displayed in nanoseconds (ns)

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Cross Clock Domains Report:
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=========================================================================


Total REAL time to Xst completion: 13.00 secs
Total CPU time to Xst completion: 13.21 secs

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Total memory usage is 275328 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings : 1581 (   0 filtered)
Number of infos    :  576 (   0 filtered)
```

8. CONCLUSION

For the LDPC codes used in low power wireless networks and wireless sensor devices, power consumption and hardware utilization are essential. This study obtained results and analyses the low power LDPC decoding architecture incorporating check node and variable node.This proposed LDPC architecture are designed and tested on various platform, its hardware utilization and power consumption are discussed with its proposed architecture**.**

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